# FERROELECTRIC CAPACITOR

## CROSS REFERENCE TO RELATED APPLICATION

A claim of priority under 35 U.S.C. §119 is made to Japanese Patent Application No. 2003-106601, filed April 10, 2003, which is herein incorporated by reference in its entirety for all purposes.

## BACKGROUND OF THE INVENTION

### FIELD OF THE INVENTION

The present invention relates to a ferroelectric capacitor.

### DESCRIPTION OF THE RELATED ART

A ferroelectric memory is a kind of nonvolatile memory. A mechanism of polarization of the ferroelectric capacitor is described in a reference 1: "Ferroelectric thin film integration technology" Tadashi Shiosaki, February 28, 1992, Science Forum Inc, pp. 205-213. Also, a device structure is described in a reference 2: Japanese Patent Laid-Open No. 5-82802 and a reference 3: Japanese Patent Laid-Open No. 2001-156263.

In a conventional ferroelectric memory, one terminal of a ferroelectric capacitor is connected to a drive line and the other terminal of the ferroelectric capacitor is connected to a bit line via a select transistor as described in reference 2. The polarized condition of the ferroelectric capacitor represents the data of a memory cell. For example, a condition that

the ferroelectric capacitor is polarized positive can represent data of "1" and a condition that the ferroelectric capacitor is polarized negative can represent data of "0".

When the drive line is high level and the select transistor turns on, a voltage of the bit line changes responsive to the polarization condition of the ferroelectric capacitor. The voltage of the bit line is amplified by a sense amplifier and outputted.

The ferroelectric memory is a destructive read type memory. Therefore, a rewriting step is needed for every read step. The rewriting step is performed by supplying the amplified voltage to the bit line.

Recently, fast read ferroelectric memories are desired. The inventor has thus considered the causes of the read time of the ferroelectric memory being slow.

Fig. 1 is a plot showing a relationship between a delay time and a read margin. The delay time shows a time from when a read voltage is applied between each of the terminals of the ferroelectric capacitor, to when the sense amplifier is operated. The read margin is a voltage difference between a read voltage representing a data "1" as stored in the ferroelectric capacitor and a read voltage representing a data "0" as stored in the ferroelectric capacitor. A high level is shown by "1" and a low level is shown by "0". In Fig. 1, a vertical axis shows the read margin and a horizontal axis shows the delay time. Fig. 1 shows cases of read voltage of 2V, 3V and 3.6V.

For example, if a margin of 0.4V is needed, a delay time is 400ns, 60ns and 40ns respectively for each read voltage 2V, 3V and 3.6V.

Fig. 2(A) to Fig. 2(C) are plots showing a relationship between a delay time and a voltage of the bit line. In Fig. 2(A) to Fig. 2(C), a vertical axis shows the voltage of the

bit line and a horizontal axis shows the delay time. A lowest voltage from the memory cell which is stored as a "1" value and a highest voltage from the memory cell which is stored as a "0" value are shown in Fig. 2(A) to Fig. 2(C). Fig. 2(A) to Fig. 2(C) show a plot for writing voltage of 2V, 3V and 3.6V respectively.

If the stored data is "1", the read voltage is dependent largely on the time. If the stored data is "0", the read voltage is not dependent so much on the time. Data "1" is read with a polarization reversal and data "0" is read without the polarization reversal. That is, the delay time is dependent on the polarization reversal time.

Fig. 3(A) and Fig. 3(B) are plots showing a relationship between the delay time and the voltage of the bit line. Fig. 3(A) shows curves of data "0" of Fig. 2(A) to Fig. 2(C), and Fig. 3(B) shows curves of data "1" of Fig 2(A) to Fig. 2(C).

If data is "0", the relationship between the delay time and the voltage of the bit line is not dependent on the read voltage. If data is "1", the relationship between the delay time and the voltage of the bit line is largely dependent on the read voltage. Therefore, using high read voltage is preferable for fast reading time of the ferroelectric capacitor.

However, using high voltage for reading the ferroelectric memory increases power consumption. If the voltage applied between each terminal of the ferroelectric capacitor is increased, field intensity at the ferroelectric capacitor is increased. As a result, reliability of the ferroelectric layer of the ferroelectric capacitor is decreased.

Fig. 4(A) to Fig. 4(C) are views showing a mechanism of the polarization of the ferroelectric capacitor. First, a voltage is applied with a bottom electrode 1201 and a top electrode 1203. Then, cores 1204 for inverting the polarization are generated in a

ferroelectric layer 1202 as shown in Fig. 4(A). The cores 1204 are generated in a boundary face between the bottom electrode 1201 and the ferroelectric layer 1202 and a boundary face between the top electrode 1203 and the ferroelectric layer 1202. Then, the cores 1204 are extended to the other electrode as shown in Fig. 4(B). Then, the cores 1204 are extended in horizontal direction and combined with each other as shown in Fig. 4(C). As a result, the inversion of the polarization of the ferroelectric capacitor is completed.

In the polarization operation, an extending speed of the cores in a vertical direction is fast, and an extending speed of the cores in a horizontal direction is slow. Therefore, a time for the polarization operation is dependent largely on the extending time in the horizontal direction.

## SUMMARY OF THE INVENTION

Accordingly, in one aspect of the present invention, a ferroelectric capacitor for reducing a reading time is provided. The ferroelectric capacitor includes a bottom electrode, a ferroelectric layer formed on the bottom electrode, and a top electrode formed on the ferroelectric layer. A plurality of projection electrodes are formed on the bottom electrode.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plot showing a relationship between delay time and read margin in a conventional ferroelectric memory.

Fig. 2(A) to Fig. 2(C) are plots showing a relationship between delay time and a voltage of the bit line in the conventional ferroelectric memory.

Fig. 3(A) and Fig. 3(B) are plots showing a relationship between delay time and the voltage of the bit line in the conventional ferroelectric memory.

Fig. 4(A) to Fig. 4(C) are views showing a mechanism of the polarization of the ferroelectric capacitor in the conventional ferroelectric memory.

Figs. 5 is a cross-sectional view showing a ferroelectric capacitor of a first embodiment of the present invention.

Fig. 6(A) to Fig. 6(D) are views showing manufacturing steps for the ferroelectric capacitor of the first embodiment of the present invention.

Fig. 7 is a plan view showing the ferroelectric capacitor of the first embodiment of the present invention.

Fig. 8 is a cross-sectional view showing the ferroelectric capacitor of the first embodiment of the present invention.

Fig. 9(A) to Fig. 9(D) are views showing manufacturing steps for a ferroelectric capacitor of a second embodiment of the present invention.

Fig. 10 (A) to Fig. 10(D) are views showing manufacturing steps for a ferroelectric capacitor of a third embodiment of the present invention.

Fig. 11(A) to Fig. 11(C) are views showing manufacturing steps for a ferroelectric capacitor of a fourth embodiment of the present invention.

Fig. 12(A) to Fig. 12(C) are views showing manufacturing steps for a ferroelectric capacitor of a fifth embodiment of the present invention.

Fig. 13(A) to Fig. 13(C) are views showing manufacturing steps for a ferroelectric capacitor of a sixth embodiment of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A ferroelectric capacitor according to preferred embodiments of the present invention will be explained hereinafter with reference to the accompanying figures. In order to simplify the explanation, like elements are given like or corresponding reference numerals. Dual explanations of the same elements are avoided.

A ferroelectric memory device 100 is described by referring to Fig. 5 to Fig. 7. Figs. 5 is a cross-sectional view showing a ferroelectric capacitor 130 of a first embodiment of the present invention. A silicon dioxide layer 120 is formed on a semiconductor substrate 110 and the ferroelectric capacitor 130 is formed on the silicon dioxide layer 120 as shown in Fig. 5. The ferroelectric capacitor 130 includes a bottom electrode 131, a plurality of projection electrodes 132 on the bottom electrode layer 131, a ferroelectric layer 133 formed on the bottom electrode layer 131, and a top electrode layer 134 formed on the ferroelectric layer 133.

The bottom electrode layer 131, the projection electrodes 132 and the top electrode layer 134 are made of platinum or iridium. Also, platinum alloy or iridium alloy can be used. Further, a laminated structure of $IrO_2$/Ir or Pt/$IrO_2$/Ir can be used.

The ferroelectric layer 133 is made of $SrBi_2Ta_2O_9$, $PbZr_xTi_{1-x}(0\leq x\leq 1)$, $PbTiO_3$ or $Bi_4Ti_3O_{12}$. A range from 5% to 20% of Ta in the $SrBi_2Ta_2O_9$ can be changed to Nb.

Next, a method of fabricating the ferroelectric capacitor 130 is described by

referring to Fig. 6(A) to Fig. 6(D).

Initially, the silicon dioxide layer 120 is formed on the silicon substrate 110 by using a plasma TEOS technique as shown in Fig. 6(A). A thickness of the silicon dioxide layer 120 is 200nm.

Then, the bottom electrode layer 131 such as platinum is formed on the silicon dioxide layer 120 by a sputtering technique as shown in Fig. 6(A). A thickness of the bottom electrode layer 131 is 200nm.

Then, a resist pattern 201 is formed on the bottom electrode layer 131 by using a photolithography technique as shown in Fig. 6(B).

Then, platinum is deposited on the entire surface of the bottom electrode layer 131 including the resist pattern 201. Then, the resist pattern 201 is removed , including the platinum portion which is formed on the resist pattern 201. As a result, the projection electrodes 132 are formed by the platinum that remains, as shown in Fig. 6(C). A thickness of the projection electrodes 132 is 10% of a thickness of the ferroelectric layer 133.

Fig. 7 is a plan view showing a layout of the projection electrodes 132. The ferroelectric capacitor 130 has a size of 5μm by 4μm. Each of the projection electrodes 132 has a size of 0.5μm in diameter. Each space between the projection electrodes 132 is 0.5μm. Each distance between centers of the projection electrodes 132 is 1μm.

For generating the polarization evenly in the ferroelectric capacitor 110, it is preferred that the projection electrodes 132 are arranged evenly on a surface of the bottom electrode layer 131.

If the projection electrodes 132 are arranged with too high a density, the polarization might not be generated evenly. Therefore, each space between the projection electrodes 132 should have a size of a range from 5% to 10% of the size of the ferroelectric capacitor 130, a size of the projection electrodes 132 should have a range from 5% to 10% of the size of the ferroelectric capacitor 130, and a distance between the center of the projection electrodes 132 should be in a range from 10% to 20% of the size of the ferroelectric capacitor 130.

Then, a ferroelectric material is formed on the bottom electrode layer 131 and the projection electrodes 132 by a spin coating technique. Then, the ferroelectric material is annealed in an oxygen atmosphere at 700°C for 60 minutes. As a result, the ferroelectric layer 133 is formed as shown in Fig. 6(D). A thickness of the ferroelectric layer 133 is 120nm.

Then, the top electrode layer 134 is formed by sputtering platinum on the ferroelectric layer as shown in Fig. 5. A thickness of the ferroelectric layer 134 is 200nm.

Next, an explanation of how the ferroelectric memory device operates is described by referring to Fig. 8.

A thickness of the ferroelectric layer which is located on the projection electrodes 132 is thinner than a thickness of the ferroelectric layer which is located on the non-projection areas of the first electrode layer 131. Therefore, electric field intensity between the projection electrodes 132 and the top electrode 134 is stronger than electric field intensity between the non-projection areas of the bottom electrode layer 131 and the top electrode 134. As a result, cores for inverting the polarization are generated between

the projection electrodes 131 and the top electrode 134. Accordingly, since the projection electrodes 132 are arranged evenly with short distance between each other, the cores for inverting the polarization are generated evenly with short distance between each other. Since the distance between the cores for inverting the polarization is short, an extending width for inverting the polarization in the horizontal direction can be reduced as shown by reference symbol "L" in Fig. 8. As a result, a time for inverting the polarization is reduced.

Next, a method of manufacturing a ferroelectric memory device of a second preferred embodiment is described by referring to Fig. 9(A) to Fig. 9(D).

First, the silicon dioxide layer 120 is formed on the silicon substrate 110 by using a plasma TEOS technique as shown in Fig. 9(A). A thickness of the silicon dioxide layer 120 is 200nm.

Then, a bottom electrode layer 401 is formed on the silicon dioxide layer 120 by using an RF sputtering technique as shown in Fig. 9(A). The material that is used as the bottom electrode layer 131 of the first embodiment can be used as the bottom electrode 401 of the second embodiment.

Then, a resist layer is formed on the bottom electrode layer 401. Then, the resist layer is patterned for making a resist pattern 402 as shown in Fig. 9(B).

Then, the bottom electrode layer 401 is etched by using the resist pattern 402 as a mask. As a result, the projection electrodes 132 are formed under the resist pattern 402 and the remaining portion becomes the bottom electrode 131. The resist pattern 402 is removed after the etching as shown in Fig. 9(C). The etching step is performed by a dry

etching technique. A thickness of the projection electrodes 132 and an arrangement of the projection electrodes 132 are the same as the thickness and the arrangement of the first embodiment.

Then, the ferroelectric layer 133 is formed on the bottom electrode 131 and the projection electrodes 132. A thickness of the ferroelectric layer 133 is 120nm.

Then, the top electrode 134 is formed on the ferroelectric layer 133 as shown in Fig. 9(D). A thickness of the top electrode 134 is 200nm.

According to the second embodiment, the projection electrodes 132 are formed by etching a surface of the bottom electrode layer 401.

Next, a ferroelectric memory device of a third preferred embodiment is described by referring Fig. To 10(A) to Fig. 10(D).

First, the silicon dioxide layer 120 is formed on the silicon substrate 110 by using a plasma TEOS technique as shown in Fig. 10(A). A thickness of the silicon dioxide layer 120 is 200nm.

Then, the bottom electrode layer 131 is formed on the silicon dioxide layer 120 by using an RF sputtering technique as shown in Fig. 10(A). The material that is used as the bottom electrode layer 131 of the first embodiment can be used as the bottom electrode 401 of the second embodiment.

Then, a resist layer is formed on the bottom electrode layer 131. Then, the resist layer is patterned for making a resist pattern 501 as shown in Fig. 10(B).

Then, bismuth is deposited on entire surface of the bottom electrode layer 131 including the resist pattern 501. Then, the resist pattern 501 is removed including the

bismuth portion which is formed on the resist pattern 501. As a result, projection electrodes 532 made of bismuth are formed as shown in Fig. 10(C). A thickness of the projection electrodes 532 is 10% of the thickness of the ferroelectric layer 133.

Then, the ferroelectric layer 133 such as $SrBi_2Ta_2O_9$ is formed on the bottom electrode 131 and the projection electrodes 532. A thickness of the ferroelectric layer 133 is 120 nm.

Then, the top electrode 134 is formed on the ferroelectric layer 133 as shown in Fig. 10(D). A thickness of the top electrode 134 is 200nm.

When the ferroelectric layer 133 is made of $SrBi_2Ta_2O_9$, the core for inverting the polarization is generated at a portion that a concentration of the bismuth is high. Also, bismuth alloy can be used as the projection electrodes 532.

When another material is used for the ferroelectric layer 133, a material that is included in the material of the ferroelectric layer 133 can be used as the material of the projection electrodes 532.

Next, a ferroelectric memory device of a fourth preferred embodiment is described by referring to Fig. 11(A) to Fig. 11(C).

First, the silicon dioxide layer 120 is formed on the silicon substrate 110 by using a plasma TEOS technique. A thickness of the silicon dioxide layer 120 is 200nm. Then, the bottom electrode 131 is formed on the silicon dioxide layer 120. Then, the ferroelectric layer 133 is formed on the bottom electrode 131. A top surface of the ferroelectric layer 133 is substantially flat.

Then, a resist layer is formed on the ferroelectric layer 133. A resist pattern 601

is formed by patterning the resist layer as shown in Fig. 11(A).

Then, bismuth is deposited on entire surface of the ferroelectric layer 133 including the resist pattern 601. Then, the resist pattern 601 is removed including the bismuth portion which is formed on the resist pattern 601. As a result, bismuth electrodes 602 are formed as shown in Fig. 11(B). A thickness of the projection electrodes 602 and an arrangement of the bismuth electrodes 602 are the same as the thickness and the arrangement of the projection electrodes 132 of the first embodiment.

Then, the top electrode 134 such as platinum is formed on the ferroelectric layer 133 and the bismuth electrodes 602 as shown in Fig. 11(C). The surfaces of the projection electrodes 602 and the surfaces of the top electrode 134 that are in contact with the ferroelectric layer 133 are substantially coplanar with respect to each other.

In this embodiment, the bismuth electrodes 602 which generate a core for inverting the polarization are embedded in the top electrode 134. When the ferroelectric layer 133 is made of $SrBi_2Ta_2O_9$, the core for inverting the polarization is generated at a portion that a concentration of the bismuth is high. Therefore, it is not necessary to project the bismuth electrodes 602 into the ferroelectric layer 133. Also, bismuth alloy can be used as the bismuth electrodes 602.

When another material is used for the ferroelectric layer 133, a material that is included in the material of the ferroelectric layer 133 can be used as the material of the bismuth electrodes 602.

Next, a ferroelectric memory device of a fifth preferred embodiment is described by referring to Fig. 12(A) to Fig. 12(C).

First, the silicon dioxide layer 120, the bottom electrode layer 131, projection electrodes 132, and the ferroelectric layer 133 are formed on the semiconductor substrate as in the first embodiment.

Then, a resist layer is formed on the ferroelectric layer 133. Then, a resist pattern 701 is formed on the ferroelectric layer 133 by patterning the resist layer as shown in Fig. 12(A). The resist pattern 701 is arranged above a region that the projection electrode 132 is not formed.

Then, the ferroelectric layer 133 is etched by using the resist pattern 701 as a mask. As a result, grooves are formed on the ferroelectric layer 133. Then, the resist pattern 701 is removed as shown in Fig. 12(B).

Then, projection electrodes 703 and the top electrode 134 are formed on the ferroelectric layer 133 by depositing platinum as shown in Fig. 12(C). The projection electrodes 703 are arranged above the projection electrodes 132.

Next, a ferroelectric memory device of a sixth preferred embodiment is described by referring to Fig. 13(A) to Fig. 13(C).

First, the silicon dioxide layer 120 and the bottom electrode layer 131 are formed on the silicon substrate 110 as in the first embodiment, as shown in Fig. 13(A).

Then, a top surface of the bottom electrode 131 is roughened as shown in Fig. 13(B). The rough surface can be made by etching the surface of the bottom electrode 131 or crystallizing the bottom electrode 131 by heating. When the bottom electrode 131 is made of platinum, the surface can be roughened by heating at 750°C for 30minutes. A distance between tops 802 of the rough surface may be in a range from 300nm to 500nm.

Then, the ferroelectric layer 133 and the top electrode 134 are formed as in the first embodiment, as shown in Fig. 13(C).

While the preferred form of the present invention has been described, it is to be understood that modifications will be apparent to those skilled in the art without departing from the spirit of the invention. The scope of the invention is to be determined solely by the following claims.